Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**1 2**

**3**

**PAD FUNCTIONS:**

1. **V +**
2. **V –**
3. **N/C**

**.042”**

**.066”**

**598 C**

**A**

**D**

**I**

**DIE ID**

**NOTE: CHIP BACK MUST BE ELECTRICALLY ISOLATED**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .005” X .008”**

**Backside Potential: ISOLATED**

**Mask Ref: 598 C**

**APPROVED BY: DK DIE SIZE .042” X .066” DATE: 1/22/19**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD592**

**DG 10.1.2**

#### Rev B, 7/19/02